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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/694,517

10/27/2003

Vadim V. Ivanov

TI-34415.2

2678

7590

07/26/2004

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EXAMINER

NGUYEN, HIEP

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

04

Office Action Summary	Application No.	Applicant(s)	
	10/694,517	IVANOV ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 20-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 20-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION***Drawings***

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitation "circuitry" in the last paragraph of claim 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Figure 4 is objected to because of the polarities of the signals applied to transistors (M20, M21, M24 and M25). These transistors are always in the OFF state because the PMOS transistors (M20) and (M21) have a positive voltage (V+) applied to their gates and the NMOS transistors (M25) and (M25) have a negative voltage (V-) applied to their gates. According to the specification, page 17, the gates of the cascode transistors M25 and M25 are connected to a reference voltage (Vref). Explanation is required.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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Claims 20-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Claim 20 is indefinite for the following reasons:

a) The recitation “first input voltage signal” on line 3, “second input voltage signal” on line 7 are indefinite because figure 4 of the presentation shows that the “first input voltage signal” and the “second input voltage signal” both have the same value (V+).

b) The recitation “circuitry for coupling a drain of the second cascode transistor to the first and second input terminals to supply the first and second input currents such that they represent the difference between the first and second input voltage signals” on line 37-39 is indefinite because the “circuitry” for coupling a drain of the second cascode transistor (M24) to the first and second input terminals is not shown in figure 4. Figure 4 shows that the first and second input terminals (the gates of transistors M20 and M21) are connected to a same voltage source (V+). There is no connection between the drain of the second cascode transistor (M24) to the first and second input terminals as recited.

Regarding claim 22, the recitations “a **first** input voltage signal” on line 3 and “a **second** input voltage signal” on line 7 are indefinite because it is misdescriptive. Figure 4 of the present application shows that both the first and second input transistors (M20, M21) receive a same input voltage signal (V_{in}+). The recitation “a first feedback circuit having a first input coupled to the drain of one of the first and second input transistors and a second input coupled to a gate of the pull up transistor, and an output coupled to a gate of the pull-down transistor” on lines 14-16 is indefinite because it is misdescriptive. Figure 2A of the present application shows that the “first feedback circuit” (13) has only one input that is connected to the gate of the pull up transistor (MP). There is no second input as recited. The recitation “the first and second input transistors” on line 15 lacks antecedent basis. Assumed that the first and second input transistors are transistors (M1) and (M2), then there is no such connection. The Applicant is requested to point out the “first and second input transistors” in the drawing. The recitation “a second feedback circuit having a first input coupled to the drain of one of the first and second and second input transistors and a second input coupled to the gate of the pull-down transistor, and an output coupled to the gate of the pull-up

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transistor” on lines 17-19 is indefinite because it is misdescriptive. The second feedback circuit (14) does not have two inputs. The recitation “first and second cascode transistors” On lines 9-10 lacks antecedent basis.

Regarding claim 24, the recitation “the first input of the second feedback is coupled to the drain of the other of the first and second input transistors by means of a **second cascode transistor**” is indefinite because it is misdescriptive. In figure 2, the second feedback circuit (14) has only one input coupled to the drain of the second input transistor (M2). There is no “second cascode transistor” seen.

Claims 21 and 23 are indefinite because of the technical deficiencies of claims 20 and 22.

Allowable Subject Matter

Claims 20-24 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claims 20-24 would be allowable because the prior art of record fails to teach or fairly suggest a CMOS comparator comprising a differential input stage, a CMOS output stage wherein, the differential input stage, comprises first, second input transistors, bias source, first and second cascode transistors connected as recited on lines 1-10; a CMOS output stage including P-channel pull up transistor, N-channel pull down transistor, P-channel third transistor, N-channel fourth transistor, first and second feedback circuits connected as recited on lines 11-27 wherein the first and second feedback circuits generates delays to prevent shoot-through current from flowing through the pull up and pull down transistors as recited in claim 20; a CMOS comparator circuit comprising a differential input stage including first and second input transistors and a bias source connected as shows on lines 1-11; a CMOS output stage including a P-channel pull up transistor and an N-channel pull down transistor, first and second feedback circuits connected as shown on lines 14-19 wherein, the feedback circuits produce delays to prevent shoot-through current from flowing through the pull up and pull down transistors as called for in claim 22.

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Conclusion

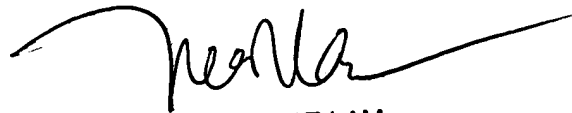
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

07-20-04



TUAN T. LAM
PRIMARY EXAMINER